REMARKS

Responsive to the Office Action mailed March 31, 2010, entry of this paper and reconsideration and allowance of the application is earnestly requested.

Status of the claims

Claims 1-31 were examined. Claims 32-37 are withdrawn.

Claims 1-4, 7, 9-11, 15-22, 24, 25, 29, and 31 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Ishinaga et al, U.S. Pat. No. 6,093,940 (hereinafter "Ishinaga").

Claim 27 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ishinaga.

Claims 5, 6, 8, 26, and 30 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ishinaga in view of Toda et al., U.S. Pat. No. 6,184,544 (hereinafter "Toda").

Claims 23 and 28 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ishinaga in view of Perduijn et al., U.S. Pat. No. 6,392,778 (hereinafter "Perduijn").

Claims 12-14 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ishinaga in view of Antle et al., U.S. Pat. No. 5,914,501 (hereinafter "Antle").

Claim amendments

Withdrawn **claims 32-37** are canceled herein. However, Applicants reserve the right to prosecute these claims in a future divisional, continuation, or continuation-in-part application.

Claim 21 is placed into independent form including all limitations of intervening base claims 1, 17, 18, and 19. *It is respectfully submitted that the scope of claims 21-25 is unaltered by this amendment.*

Claim 1 is amended to recite a lead frame attached to the top principal surface of the chip carrier but not to the bottom principal surface of the chip carrier. This amendment is clarifying in nature, and finds support in the original specification at least in the lead frame (40, 42), lead frame (140, 142), lead frame (340, 342), and lead frame (440, 442) shown in respective Figs. 1, 2B, 4C, and 5C, and related text.

New **claim 38** includes all subject matter of original claim 17 (both of which depend from claim 1), and further recites electrical leads being shaped to include lead portions distal from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier. Support for the additional subject matter is found in the original specification at least at page 4 lines 15-18.

New **claim 39** is an independent claim including subject matter of original claim 1 and new claim 38.

New **claims 40 and 41** depends from claims 1 and 39, respectively, and recite solder bonds attaching the lead frame to the top principal surface of the chip carrier. These claims are supported in the original specification at least by solder bonds (54, 56) and at page 4 lines 18-20.

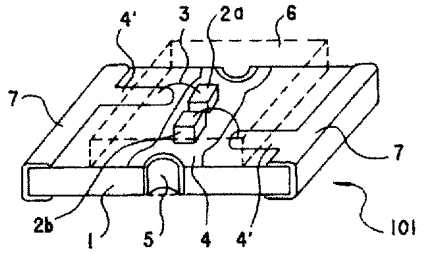
The claims present patentable subject matter and should be allowed

Claim 21 recites a light emitting package comprising: a chip carrier having top and bottom principal surfaces; at least one light emitting chip attached to the top principal surface of the chip carrier; a lead frame attached to the top principal surface of the chip carrier, the lead frame having electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier; wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame and the chip carrier, light emitting chip, and lead frame define a surface mountable unit; a printed circuit board on which the printed circuitry is disposed, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry, the bottom principal surface of the chip carrier being in direct contact with the printed circuit board.

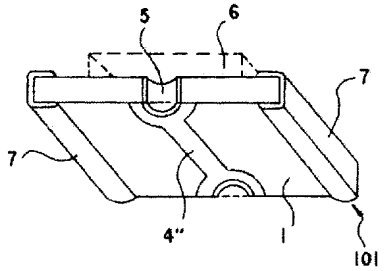
The Office Action alleges claim 21 is anticipated by Ishinaga. Applicants respectfully traverse the §102 rejection, and further argue that claim 21 is not obvious in view of Ishinaga.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior reference. MPEP § 2131. The identical invention must be shown in as complete detail as is contained in the claim. *Id.* The elements must be arranged as required by the claim (although identity of terminology is not required). *Id.*

Claim 21 recites a chip carrier having top and bottom principal surfaces and at least one light emitting chip attached to the top principal surface of the chip carrier. In Ishinaga Fig. 1 shows a substrate (1) with a principal surface at which at least one light emitting chip (namely two LED elements (2a, 2b)) are attached, thus identifying a "top principal surface" for the substrate (1).

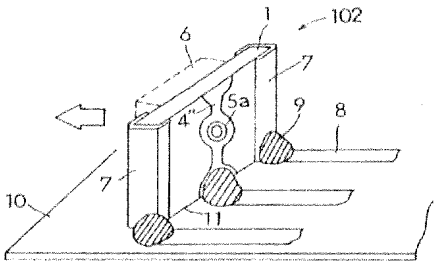


Ishinaga Fig. 1 also shows the (thereby identified) bottom principal surface:



Claim 21 further recites a printed circuit board on which the printed circuitry is disposed, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry, *the bottom principal surface of the chip carrier being in direct contact with the printed circuit board.*

In rejecting this subject matter, the Office Action cites Ishinaga Fig. 7 and col. 5 lines 40-55. Office Action page 8. Cited Fig. 7 is reproduced below:



This illustrates an *edge-mounted* configuration in which the bottom surface is visible facing to the right, and *not* in direct contact with the printed circuit board (10). Indeed, such an edge-mounting so as to provide side-surface light emission is the primary object of Ishinaga. Ishinaga col. 5 lines 43-44. Moreover, even if one were to reorient the LED chip component (102) with the bottom surface facing the circuit board (10), the result would *not* be the bottom principal surface of the chip carrier being in direct contact with the printed circuit board; rather, the terminal patterns (7) would intervene between the bottom surface of the substrate (1) and the circuit board (10), thus preventing direct contact with the printed circuit board.

Claim 21 further recites the lead frame having electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, *the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier*. Ishinaga, in contrast, discloses its terminal patterns (7) having portions passing *underneath* the substrate (1), not shaped to include lead portions *approximately coplanar with* the bottom principal surface of the chip carrier.

The foregoing is sufficient to establish that claim 21 is *not anticipated* by Ishinaga. It is further respectfully submitted that claim 21 is *not obvious* in view of Ishinaga. As the present application (*not* Ishinaga) discloses, "Such arrangements [as in Ishinaga] have certain disadvantages. The thermal transfer path includes two intervening elements, namely the sub-mount and the lead frame."

Present application page 1 lines 15-17. Claim 21 (*not* Ishinaga) recites a solution to this problem which includes a lead frame attached to the *top* principal surface of the chip carrier, the electrical leads being shaped to include lead portions *approximately coplanar with* the bottom principal surface of the chip carrier, with the *bottom* principal surface of the chip carrier being in direct contact with the printed

circuit board. This arrangement ensures that the leads can be soldered to the circuit board as desirable for a surface-mount package, while still enabling the bottom principal surface of the chip carrier to be in direct contact with the printed circuit board so as to provide a direct thermal pathway through the chip carrier from the light emitting chip or chips to the printed circuit board.

Ishinaga does not remotely suggest such an arrangement. Indeed, Ishinaga is directed to an edge-mounted device, so as to provide side-surface light emission is the primary object of Ishinaga. Ishinaga col. 5 lines 43-44. The only mention of a "top-surface" arrangement (Ishinaga's terminology) is at col. 2 lines 1-5. The referenced device is shown in Ishinaga Figs. 10A and 10B, which in the "top-surface" arrangement would include metal patterns (4a, 4b, 4a', 4b') interposed *between* the substrate (1) and the circuit board.

Claim 24 depends from claim 21, and further recites an attachment between the lead portions contacting the printed circuitry *is different from an attachment of* the bottom principal surface of the chip carrier contacting the printed circuit board. As already noted respective to base claim 21, Ishinaga does not disclose or fairly suggest the bottom principal surface of the chip carrier being attached to the circuit board *at all*, much less using a *different attachment* from an attachment of the terminal patterns (4, 7). Indeed, Ishinaga discloses only a *single* attachment, namely the solder (9), for attaching the *terminal patterns* to the circuit board, and discloses no attachment of the *substrate* (1) to the circuit board.

At this point, Applicants wish to clarify **claim 23**, which is the basis of the specification objection. Office Action page 3. This objection appears to be a consequence of a misreading of claim 23, which does *not* recite the solder connection to the printed circuit board not being conductive.

Claim 23 actually recites the chip carrier is soldered to the printed circuit board, said soldered connection being thermally conductive *but not conducting electrical current when the light emitting chip is operated.* The specification discloses how this is achieved as follows:

> The printed traces also includes *a thermal terminal **84** which optionally is not connected with the electrical circuitry.* The bottom principal surface **50** of the

> chip carrier **14** is preferably soldered or otherwise bonded to the thermal terminal **84** to provide a substantially thermally conductive pathway therebetween, so that heat generated in the light emitting chip **12** can conduct through the substantially thermally conductive chip carrier **14** to the thermal terminal **84** and thence to the printed circuit board **70**. Optionally, the bottom principal surface **50** of the chip carrier **14** includes a metal layer for solder attach to the board or other coating to enhance thermal contact and heat transfer.
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> Present application page 5 lines 9-18 (italics added).

Thus, in embodiments in which the thermal terminal is not connected with the electrical circuitry, the soldered connection is thermally conductive (and, indeed, is electrically conductive) but does *not* conduct electrical current when the light emitting chip is operated. (By analogy, the anode and cathode of a battery can be connected with wires that are electrically conductive, but unless those wires are somehow interconnected to form a closed circuit, the wires will not conduct electrical current).

Accordingly, Applicants respectfully traverse the specification objection.

Claim 1 is amended to recite a lead frame attached to the top principal surface of the chip carrier but not to the bottom principal surface of the chip carrier. In contrast, Ishinaga's terminal patterns (4, 7) are disposed over *both* the top and bottom principal surfaces of Ishinaga's substrate (1). Moreover, as seen in Ishinaga Fig. 7 and related text (e.g., col. 6 lines 17-33), this configuration is affirmatively taught by Ishinaga as enabling achievement of Ishinaga's desired side-mounting.

New **claim 38** depends from claim 1, and recites the electrical leads being shaped to include *lead portions distal from the chip carrier* that are approximately coplanar with the bottom principal surface of the chip carrier. New **claim 39** recites the electrical leads being shaped to include *lead portions extended away from the chip carrier* that are approximately coplanar with the bottom principal surface of the chip carrier.

In contrast, no portion of Ishinaga's terminal patterns (4, 7) are distal from or extended away from the chip carrier. Ishinaga's terminal patterns (4, 7) wrap around the substrate (1), or are otherwise coated on or fitted onto the substrate (1) in an intimate fashion. *See, e.g.* Ishinaga col. 4 lines 23-30. There is no disclosure or even

fair suggestion in Ishinaga that these patterns (4, 7) include a portion that is distal from or extended away from the substrate (1).

New **claims 40 and 41** each recite solder bonds attaching the lead frame to the top principal surface of the chip carrier. Again, Ishinaga's terminal patterns (4, 7) appear to be coatings or fittings disposed on the substrate (1). There is no disclosure or even fair suggestion in Ishinaga that these patterns (4, 7) be attached to the substrate (1) by solder bonds.

For at least the reasons set forth above, it is submitted that claims 1-31 and 38-41 (all claims) present patentable subject matter and meet all statutory requirements. Accordingly, Applicants earnestly request reconsideration and allowance of the application including claims 1-31 and 38-41.

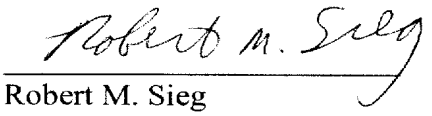
CONCLUSION

For at least the reasons set forth above, it is submitted that claims 1-31 and 38-41 (all claims) present patentable subject matter and meet all statutory requirements. Accordingly, Applicants earnestly request reconsideration and allowance of the application including claims 1-31 and 38-41.

If personal contact is deemed advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned at 216.363.9000.

Respectfully submitted,

FAY SHARPE LLP



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